Confirmation No. 2306

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	AVERY *et al.*	Examiner:	Tu, C.
Serial No.:	10/796,480	Group Art Unit:	2117
Filed:	March 8, 2004	Docket No.:	US030080 US
Title:	CIRCUIT CONFIGURATOR ARRANGEMENT AND APPROACH THEREFOR		

REPLY BRIEF

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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
65913

Dear Sir:

This Reply Brief is submitted pursuant to 37 C.F.R. § 41.41(a)(1) for the above-referenced patent application. On September 26, 2007, the Examiner issued an Examiner's Answer to Appellant's Amended Appeal Brief submitted on June 5, 2007, in support of the Notice of Appeal filed on December 29, 2006, and in response to the final rejections of claims 1-29 as set forth in the final Office Action dated October 13, 2006.

No fee should be required for the timely filing of this Reply Brief. However, if deemed necessary, authorization is given to charge/credit Deposit Account No. 50-0996 (NXPS.216PA) for all required fees/overages.

Status of Claims

Claims 1-10, 13-14, 16-18, 22-26 and 29 stand presently rejected and are presented for appeal; a complete listing of the pending claims (and those under appeal) are listed in the attached Claims Appendix, with claim status identifiers.

Grounds of Rejection As Amended by Examiner's Answer

On page 10 of the Examiner's Answer dated September 26, 2007, the 35 U.S.C. § 112(2) rejections of claims 1-29, and of claim 9 were withdrawn.

On page 17-18 of the Examiner's Answer, the provisional, nonstatutory obvious-type, double-patenting rejections of claims 1-2, 4, 8, 14-17, 23, 26-27 and 29 were withdrawn.

Therefore, Appellant respectfully requests notification that claims 11-12, 15, 19 and 27-28 are allowed, pursuant to the Examiner's reversal of the Section 112 rejections, and the provisional, obvious-type, double-patenting rejections.

Therefore, only one ground of rejection (35 U.S.C. § 103(a)) remains under this appeal, as adjudged in the Examiner's Answer dated September 26, 2007 and as identified below.

1. Claims 1-10, 13-14, 16-18, 22-26 and 29 stand rejected under 35 U.S.C. § 103(a) over Garreau (U.S. Patent No. 6,425,101).

Appellant's Reply Arguments

The sole remaining rejection, of claims 1-10, 13-14, 16-18, 22-26 and 29 over Garreau, must be reversed because the rejection relies upon an interpretation of claimed limitations as "intended use" that is in direct contrast with the M.P.E.P. and relevant law, and further because the Garreau reference does not correspond to the claimed limitations as asserted by the Examiner.

Beginning with the scope of the claims, the Examiner has asserted globally that "the use of the preposition 'to' (after an element and before a verb) creates 'intended use' limitations" and further that similar limitations including phrases such as "adapted to" create such intended use limitations as well, without providing any support whatsoever for these assertions. This assertion is wrong in that it contradicts M.P.E.P. §2111.04 and thousands of issued patents using these and similar phrases in the claimed limitations (*i.e.*, not simply in a claim preamble). For instance, M.P.E.P.§2111.04 references terms such as "adapted to" and others similar to those discussed by the Examiner, but requires that such language does not limit claim scope when the language "suggests or makes optional but does not require steps to be performed." M.P.E.P.§2111.04 goes on to indicate that a term that states a condition that is material to patentability "cannot be ignored in order to change the substance of the invention" (citing In Hoffer v. Microsoft Corp., 405 F.3d 1326, 1329, 74 USPQ2d 1481, 1483 (Fed. Cir. 2005)).

In this instance, the claimed limitations that the Examiner has determined to be "merely a statement of intended use" are as follows: "a test-signal sense circuit to detect test signals carried by at least one of the test signal routing paths"; "a switch-control interface circuit to control the controllable switches"; and "a control logic circuit to send control signals to the switch-control interface circuit." Clearly, the limitations after the preposition "to" cannot be ignored as, in each instance, the function that the respective circuits perform is specified in the claims and supported in the specification in detail. For instance, the "test-signal sense circuit" must have structure that enables it to detect test signals carried by at least one test signal routing path. In this regard, the rejections that rely upon this inappropriate reading of the preposition "to" as providing only intended use limitations are inappropriate and must be reversed.

Regarding the Garreau reference, several alleged teachings fail to provide correspondence to various claim limitations. For brevity at this (Reply Brief) stage, this

discussion focuses upon the Examiner's key misinterpretation of the function and implementation of the claimed test signal sense circuit and corresponding routing, in citing to unrelated portions of the Garreau reference that fail to teach or suggest the claimed limitations. As all of the claims rely upon this misinterpretation, all rejections (each of which is based upon the Garreau reference) must be reversed.

Generally, Garreau does not disclose controllable switches or their corresponding control as relevant to the presence of test signals detected by a test signal sense circuit as claimed in the instant invention. This claimed approach is useful for sensing the connectivity of various circuit components such as ICs and the corresponding routing of test signals therebetween. Garreau describes no automatic sensing and switching, apparently relying upon manual approaches that suffer difficulties as described, for example, in the background of the instant application. The Examiner has acknowledged that the Garreau reference "does not explicitly teach the controllable switches" at page 7 of the Final Office Action, yet has to date provided no reference that teaches or suggests these limitations, despite attempts by the Appellant to point out this lack of teaching in the record. The Examiner's Answer provides no further evidence of any prior art that teaches or suggests these limitations, and again relies upon unsupported assertions (*e.g.*, of what Garreau's JTAG controller "should" perform, and how the sensing of the completion of a test "would have lead the master controller (202) to send instructions" as recited at page 12). It is further unclear as to how sensing the completion g of a test would be useful to Garreaus's JTAG controller 210 (and master controller 202), as it is Garreau's controller that carries out the test (*i.e.*, Garreau's controller would already "know" when its test was finished). The Examiner's test completion sensing approach also stops short of describing any other sensing functions as claimed, such as those involving the monitoring of a plurality of operational characteristics of configurable test signal routing paths (*see, e.g.*, claim 8). Without support from the prior art and where Garreau would not benefit from the "completion" sensing relied upon by the Examiner, these assertions of what "should" or "would" happen are insufficient to maintain the Section 103 rejections.

VIII. Conclusion

In view of the above, Appellant submits that the Section 103(a) rejection of claims 1-10, 13-14, 16-18, 22-26 and 29 is improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this reply brief.

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CLAIMS APPENDIX
(S/N 10/796,480)

1. (previously presented) For use in controlling routing circuitry having configurable test signal routing paths with controllable switches therein for coupling test signals between dedicated test-signal circuitry and a target circuit device, a circuit configurator arrangement comprising:

a test-signal sense circuit to detect test signals carried by at least one of the test signal routing paths;

a switch-control interface circuit to control the controllable switches; and

a control logic circuit to send control signals to the switch-control interface circuit, in response to the detected test signals carried by said at least one of the test signal routing paths, and therein control routing of test signals in the configurable test signal routing paths.

2. (Original) The circuit configurator arrangement of claim 1, further comprising a communications link adapted to communicatively couple the control logic circuit to an external user-controlled device for passing reconfiguration-control signals to the control logic circuit, the control logic circuit being adapted to respond to the reconfiguration-control signals by sending control signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

3. (Original) The circuit configurator arrangement of claim 2, further comprising a memory adapted to store the reconfiguration-control signals for access by the control logic circuit, the stored reconfiguration-control signals, when executed, causing the control logic to send control signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

4. (Original) The circuit configurator arrangement of claim 2, wherein the communications link is further adapted for reporting characteristics of the configured test signal routing paths to the external user-controlled device.

5. (Original) The circuit configurator arrangement of claim 1, further comprising a memory adapted to store said control signals for access by the control logic circuit, the stored control signals, when executed, causing the control logic to send signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

6. (Original) The circuit configurator arrangement of claim 1, wherein the test-signal sense circuit is adapted to detect test signals passing between the configurable test signal routing paths and an external circuit and wherein the control logic circuit is adapted to adaptively control routing of test signal between the configurable test signal routing paths and the external circuit, in response to the detected test signals.

7. (Original) The circuit configurator arrangement of claim 1, wherein the dedicated test-signal circuitry includes a test-data input port adapted to receive test data, a test-data output port adapted to pass test data from the dedicated test-signal circuitry and a test-clock port.

8. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is programmed to control and monitor a plurality of operational characteristics of the configurable test signal routing paths.

9. (Original) The circuit configurator arrangement of claim 1, wherein the configurable test signal routing paths include a plurality of JTAG signal path switches adapted to route JTAG signals on the routing circuitry and between the routing circuitry and an external circuit, and wherein the control logic circuit is programmed to send the control signals to configure the plurality of JTAG signal path switches.

10. (Original) The circuit configurator arrangement of claim 9, wherein the control logic circuit is programmed to switch the plurality of JTAG signal path switches in response to reconfiguration-control signals received from an external user-controlled device.

11. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is adapted to monitor operational characteristics of the routing circuitry prior to power-up of the routing circuitry.

12. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is adapted to send control signals to the switch-control interface circuit and therein set the controllable switches, prior to power-up of the routing circuitry.

13. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is further adapted to control a JTAG controller for generating JTAG test signals and adaptively control the routing of the generated JTAG test signals in the configurable test signal routing paths.

14. (previously presented) For use with a configured circuit having a plurality of controllable switches communicatively coupled between at least two JTAG test nodes on JTAG signal paths and target circuit devices along the JTAG signal paths, a circuit configurator arrangement comprising:

a communications port to accept control inputs from a user interface via a communications link and to provide output data to the user via the communications link;

a test-signal sense circuit to detect JTAG test signals carried by at least one of the test signal routing paths;

a memory having computer-executable code; and

a programmable microcontroller communicatively coupled to the configured circuit, the communications port and the test signal sense circuit, wherein the computer-executable code, when executed, causes the microcontroller to control the controllable switches for coupling JTAG test signals to the target circuit devices in response to test signals sensed by the test-signal sense circuit, and to monitor operational characteristics of the configured circuit and output data to the user interface in response to the monitored operational characteristics.

15. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to cause the test-signal sense circuit to monitor the JTAG test nodes using an interrupt routine for automatically detecting test signals at the JTAG test nodes.

16. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to control the controllable switches for routing JTAG test data between the configured circuit and an external configured circuit, via the JTAG test nodes.

17. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is adapted to control the controllable switches in response to control inputs received from the user interface via the communications port.

18. (Original) The circuit configurator arrangement of claim 14, wherein the circuit configurator arrangement is adapted to receive computer-executable code from the user interface via the communications port and to store the computer-executable code in the memory, the received and stored computer-executable code, when executed, causing the microcontroller to control the controllable switches.

19. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to perform diagnostic testing on the configured circuit when the configured circuit is not powered and to report the results of the diagnostic testing via the communications port.

20. (Original) The circuit configurator arrangement of claim 19, wherein the microcontroller is programmed to report an error signal in response to the diagnostic testing indicating an error in the routing circuitry.

21. (Original) The circuit configurator arrangement of claim 19, wherein the microcontroller is adapted to perform diagnostic testing on timing circuits coupled to the routing circuitry by

detecting clock frequency thereof and, in response to detecting an improper clock frequency, to report an error signal indicating a timing error.

22. (Original) The circuit configurator arrangement of claim 14, further comprising an analog-to-digital converter (ADC) coupled to the configured circuit and adapted for converting detected analog signals thereon to digital signals, the microcontroller being further adapted for reporting characteristics of the configured circuit in response to the digital signals.

23. (previously presented) For use in a prototype arrangement of inter-connectable circuit boards, each of the inter-connectable circuit boards having JTAG test signal routing switches, at least two JTAG circuit paths and JTAG input/output (I/O) test nodes for passing JTAG test signals to and from other inter-connectable circuit boards, a configurator circuit comprising:

a memory to store data including computer-executable code;

a microcontroller on a first one of the inter-connectable circuit boards and communicatively coupled to the memory, the computer-executable code, when executed, causing the microcontroller to:

monitor the JTAG I/O test nodes to detect connectivity to another inter-connectable circuit; and

automatically configure the JTAG test signal routing switches in response to the JTAG I/O test node monitoring for routing JTAG test signals along a JTAG circuit path on at least the first one of the inter-connectable circuit boards; and

a communications link to communicate control inputs from a user interface device to the microcontroller and to communicate outputs from the microcontroller to the user interface, the microcontroller being operable in response to the control inputs.

24. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to monitor the JTAG I/O test nodes and, in response to detecting connectivity to another inter-connectable circuit via the monitoring, to set the controllable switches for routing JTAG test signals between the inter-connectable circuits.

25. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to monitor the JTAG I/O test nodes and, in response to detecting that another inter-connectable circuit is not connected to a particular JTAG test node via the monitoring, to set the controllable switches for routing away from the particular JTAG test node.

26. (Original) The configurator circuit of claim 23, wherein the microcontroller is adapted to set the JTAG test signal routing switches in response to control inputs received from the user interface.

27. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to perform an interrupt routine for monitoring the JTAG I/O test nodes.

28. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to perform a data-polling routine for monitoring the JTAG I/O test nodes.

29. (previously presented) For use in controlling routing circuitry having configurable test signal routing paths with controllable switches therein for coupling test signals between dedicated test-signal circuitry and a target circuit device, a circuit configurator arrangement comprising:

test-signal sensing means for detecting test signals carried by at least one of the test signal routing paths;

switch-control interface means for controlling the controllable switches; and

control logic means for sending control signals to the switch-control interface circuit, in response to the detected test signals carried by said at least one of the test signal routing paths, and therein control routing of test signals in the configurable test signal routing path.